On Chip Communication Architectures System On Chip Interconnect Systems On Silicon

ICCAD serves EDA and design professionals, highlighting new challenges and innovative solutions for integrated circuit design technology and systems

This textbook aims to provide learners with an understanding of embedded systems built around Arm Cortex-M processor cores, a popular CPU architecture often used in modern low-power SoCs that target IoT applications. Readers will be introduced to the basic principles of an embedded system from a high-level hardware and software perspective and will then be taken through the fundamentals of microcontroller architectures and SoC-based designs. Along the way, key topics such as chip design, the features and benefits of Arm's Cortex-M processor architectures (including TrustZone, CMSIS and AMBA), interconnects, peripherals and memory management are discussed. The material covered in this book can be considered as key background for any student intending to major in computer engineering and is suitable for use in an undergraduate course on digital design.

A Multi-Processor System-on-Chip (MPSoC) is the key component for complex applications. These applications put huge pressure on memory, communication devices and computing units. This book, presented in two volumes – Architectures and Applications – therefore celebrates the 20th anniversary of MPSoC, an interdisciplinary forum that focuses on multi-core and multi-processor hardware and software systems. It is this interdisciplinarity which has led to MPSoC bringing together experts in these fields from around the world, over the last two decades. Multi-Processor System-on-Chip 2 covers application-specific MPSoC design, including compilers and architecture exploration. This second volume describes optimization methods, tools to optimize and port specific applications on MPSoC architectures. Details on compilation, power consumption and wireless communication are also presented, as well as examples of modeling frameworks and CAD tools. Explanations of specific platforms for automotive and real-time computing are also included.

This book provides a comprehensive survey of recent progress in the design and implementation of Networks-on-Chip. It addresses a wide spectrum of on-chip communication problems, ranging from physical, network, to application layers. Specific topics that are explored in detail include packet routing, resource arbitration, error control/correction, application mapping, and communication scheduling. Additionally, a novel bi-directional communication channel NoC (BiNoC) architecture is described, with detailed explanation. Written for practicing engineers in need of practical knowledge about the design and implementation of networks-on-chip; Includes tutorial-like details to introduce readers to a diverse range of NoC designs, as well as in-depth analysis for designers with NoC experience to explore advanced issues; Describes a variety of on-chip communication architectures, including a novel bi-directional communication channel NoC. From the Foreword: Overall this book shows important advances over the state of the art that will affect future system design as well as R&D in tools and methods for NoC design. It represents an important reference point for both designers and electronic design automation researchers and developers. --Giovanni De Micheli

"This book is on the topic of reconfigurable network-on-chip, which is a culmination of growing trends in the two hot research areas, namely reconfigurable computing and network-on-chip"--Provided by publisher.

Traditionally, design space exploration for Systems-on-Chip (SoCs) has focused on the computational aspects of the problem at hand.

However, as the number of components on a single chip and their performance continue to increase, the communication architecture plays a major role in the area, performance and energy consumption of the overall system. As a result, a shift from computation-based to communication-based design becomes mandatory. Towards this end, network-on-chip (NoC) communication architectures have emerged recently as a promising alternative to classical bus and point-to-point communication architectures. In this dissertation, we study outstanding research problems related to modeling, analysis and optimization of NoC communication architectures. More precisely, we present novel design methodologies, software tools and FPGA prototypes to aid the design of application-specific NoCs.

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years

The purpose of this book is to evaluate strategies for future system design in multiprocessor system-on-chip (MPSoC) architectures. Both hardware design and integration of new development tools will be discussed. Novel trends in MPSoC design, combined with reconfigurable architectures are a main topic of concern. The main emphasis is on architectures, design-flow, tool-development, applications and system design.

Going beyond isolated research ideas and design experiences, Designing Network On-Chip Architectures in the Nanoscale Era covers the foundations and design methods of network on-chip (NoC) technology. The contributors draw on their own lessons learned to provide strong practical guidance on various design issues. Exploring the design process of the network, the first part of the book focuses on basic aspects of switch architecture and design, topology selection, and routing implementation. In the second part, contributors discuss their experiences in the industry, offering a roadmap to recent products. They describe Tilera's TILE family of multicore processors, novel Intel products and research prototypes, and the TRIPS operand network (OPN). The last part reveals state-of-the-art solutions to hardware-related issues and explains how to efficiently implement the programming model at the network interface. In the appendix, the microarchitectural details of two switch architectures targeting multiprocessor system-on-chips (MPSoCs) and chip multiprocessors (CMPs) can be used as an experimental platform for running tests. A stepping stone to the evolution of

future chip architectures, this volume provides a how-to guide for designers of current NoCs as well as designers involved with 2015 computing platforms. It cohesively brings together fundamental design issues, alternative design paradigms and techniques, and the main design tradeoffs—consistently focusing on topics most pertinent to real-world NoC designers.

This book presents an overview of the issues related to the test, diagnosis and fault-tolerance of Network on Chip-based systems. It is the first book dedicated to the quality aspects of NoC-based systems and will serve as an invaluable reference to the problems, challenges, solutions, and trade-offs related to designing and implementing state-of-the-art, on-chip communication architectures.

The first book to survey this emerging field in digital system design.

Abstract: Network-on-Chip (NoC) communication architectures have been recognized as the most scalable and efficient solution for on chip communication challenges in the multi-core era. Diverse demanding applications coupled with the ability to integrate billions of transistors on a single chip are some of the main driving forces behind ever increasing performance requirements towards the level that requires several tens to over a hundred of cores per chip. Small scale multicore processors so far have been a great commercial success and found applicability in many applications. Systems using multi-core processors are now the norm rather than the exception. As the number of cores or components integrated into a single system is keep increasing, the design of on-chip communication architecture is becoming more challenging. The increasing number of components in a system translates into more inter-component communication that must be handled by the on-chip communication infrastructure. Future system-on-chip (SoC) designs require predictable, scalable and reusable on-chip communication architectures to increase reliability and productivity. Current bus-based interconnect architectures are inherently non-scalable, less adaptable for reuse and their reliability decreases with system size. NoC communication guarantees scalability, high-speed, high-bandwidth communication with minimal wiring overhead and routing issues. NoCs are layered, packet-based on-chip communication networks integrated onto a single chip. NoC consists of resources and switches that are directly connected in a way that resources are able to communicate with each other by sending messages. The proficiency of a NoC to meet its design goals and budget requirements for the target application depends on its design. Often, these design goals conflict and trade-off with each other. The multi-dimensional pull of design constraints in addition to technology scaling complicates the process of NoC design in many aspects, as they are expected to support high performance and reliability along with low cost, smaller area, less time-to-market and lower power consumption. To aid in the process, this research presents design methodologies to achieve low power and high performance NoC communication architectures for nanometer SoCs.

A Multi-Processor System-on-Chip (MPSoC) is the key component for complex applications. These applications put huge pressure on memory, communication devices and computing units. This book, presented in two volumes – Architectures and Applications – therefore celebrates the 20th anniversary of MPSoC, an interdisciplinary forum that focuses on multi-core and multi-processor hardware and software systems. It is this interdisciplinarity which has led to MPSoC bringing together experts in these fields from around the world, over the last two decades. Multi-Processor System-on-Chip 1 covers the key components of MPSoC: processors, memory, interconnect and interfaces. It describes advance features of these components and technologies to build efficient MPSoC architectures. All the main components are detailed: use of memory and their technology, communication support and consistency, and specific processor architectures for general purposes or for dedicated applications.

Intelligent readers who want to build their own embedded computer systems-- installed in everything from cell phones to cars to handheld organizers to refrigerators-- will find this book to be the most in-depth, practical, and up-to-date guide on the market. Designing Embedded Hardware carefully steers between the practical and philosophical aspects, so developers can both create their own devices and gadgets and customize and extend off-the-shelf systems. There are hundreds of books to choose from if you need to learn programming, but only a few are available if you want to learn to create hardware. Designing Embedded Hardware provides software and hardware engineers with no prior experience in embedded systems with the necessary conceptual and design building blocks to understand the architectures of embedded systems. Written to provide the depth of coverage and real-world examples developers need, Designing Embedded Hardware also provides a road-map to the pitfalls and traps to avoid in designing embedded systems. Designing Embedded Hardware covers such essential topics as: The principles of developing computer hardware Core hardware designs Assembly language concepts Parallel I/O Analog-digital conversion Timers (internal and external) UART Serial Peripheral Interface Inter-Integrated Circuit Bus Controller Area Network (CAN) Data Converter Interface (DCI) Low-power operation This invaluable and eminently useful book gives you the practical tools and skills to develop, build, and program your own application-specific computers.

Networks-on-Chip: From Implementations to Programming Paradigms provides a thorough and bottom-up exploration of the whole NoC design space in a coherent and uniform fashion, from low-level router, buffer and topology implementations, to routing and flow control schemes, to co-optimizations of NoC and high-level programming paradigms. This textbook is intended for an advanced course on computer architecture, suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture and Networks-on-Chip. It is also intended for practitioners in the industry in the area of microprocessor design, especially the many-core processor design with a

network-on-chip. Graduates can learn many practical and theoretical lessons from this course, and also can be motivated to delve further into the ideas and designs proposed in this book. Industrial engineers can refer to this book to make practical tradeoffs as well. Graduates and engineers who focus on off-chip network design can also refer to this book to achieve deadlock-free routing algorithm designs. Provides thorough and insightful exploration of NoC design space. Description from low-level logic implementations to co-optimizations of high-level program paradigms and NoCs. The coherent and uniform format offers readers a clear, quick and efficient exploration of NoC design space Covers many novel and exciting research ideas, which encourage researchers to further delve into these topics. Presents both engineering and theoretical contributions. The detailed description of the router, buffer and topology implementations, comparisons and analysis are of high engineering value.

This book provides a broad overview of current research in optical interconnect technologies and architectures. Introductory chapters on high-performance computing and the associated issues in conventional interconnect architectures, and on the fundamental building blocks for integrated optical interconnect, provide the foundations for the bulk of the book which brings together leading experts in the field of optical interconnect architectures for data communication. Particular emphasis is given to the ways in which the photonic components are assembled into architectures to address the needs of data-intensive on-chip communication, and to the performance evaluation of such architectures for specific applications.

System on chips designs have evolved from fairly simple unicore, single memory designs to complex heterogeneous multicore SoC architectures consisting of a large number of IP blocks on the same silicon. To meet high computational demands posed by latest consumer electronic devices, most current systems are based on such paradigm, which represents a real revolution in many aspects in computing. The attraction of multicore processing for power reduction is compelling. By splitting a set of tasks among multiple processor cores, the operating frequency necessary for each core can be reduced, allowing to reduce the voltage on each core. Because dynamic power is proportional to the frequency and to the square of the voltage, we get a big gain, even though we may have more cores running. As more and more cores are integrated into these designs to share the ever increasing processing load, the main challenges lie in efficient memory hierarchy, scalable system interconnect, new programming paradigms, and efficient integration methodology for connecting such heterogeneous cores into a single system capable of leveraging their individual flexibility. Current design methods tend toward mixed HW/SW co-designs targeting multicore systems on-chip for specific applications. To decide on the lowest cost mix of cores, designers must iteratively map the device's functionality to a particular HW/SW partition and target architectures. In addition, to connect the heterogeneous cores, the architecture requires high performance complex communication architectures and efficient communication protocols, such as hierarchical bus, point-to-point connection, or Network-on-Chip. Software development also becomes far more complex due to the difficulties in breaking a single

processing task into multiple parts that can be processed separately and then reassembled later. This reflects the fact that certain processor jobs cannot be easily parallelized to run concurrently on multiple processing cores and that load balancing between processing cores – especially heterogeneous cores – is very difficult.

This book describes analytical models and estimation methods to enhance performance estimation of pipelined multiprocessor systems-on-chip (MPSoCs). A framework is introduced for both design-time and run-time optimizations. For design space exploration, several algorithms are presented to minimize the area footprint of a pipelined MPSoC under a latency or a throughput constraint. A novel adaptive pipelined MPSoC architecture is described, where idle processors are transitioned into low-power states at run-time to reduce energy consumption. Multi-mode pipelined MPSoCs are introduced, where multiple pipelined MPSoCs optimized separately are merged into a single pipelined MPSoC, enabling further reduction of the area footprint by sharing the processors and communication buffers. Readers will benefit from the authors' combined use of analytical models, estimation methods and exploration algorithms and will be enabled to explore billions of design points in a few minutes.

Such a multi-faceted synthesis framework accrues many benefits for MPSoC designs such as improved design reliability and quality, better complexity management, reduced system cost and a faster time-to-market. The experiments on several industrial strength applications demonstrate the utility of the automated and comprehensive synthesis framework for MPSoC designs.

System on Chip Interfaces for Low Power Design provides a top-down understanding of interfaces available to SoC developers, not only the underlying protocols and architecture of each, but also how they interact and the tradeoffs involved. The book offers a common context to help understand the variety of available interfaces and make sense of technology from different vendors aligned with multiple standards. With particular emphasis on power as a factor, the authors explain how each interface performs in various usage scenarios and discuss their advantages and disadvantages. Readers learn to make educated decisions on what interfaces to use when designing systems and gain insight for innovating new/custom interfaces for a subsystem and their potential impact. Provides a top-down guide to SoC interfaces for memory, multimedia, sensors, display, and communication Explores the underlying protocols and architecture of each interface with multiple examples Guides through competing standards and explains how different interfaces might interact or interfere with each other Explains challenges in system design, validation, debugging and their impact on development

Architecture of Network Systems explains the practice and methodologies that will allow you to solve a broad range of problems in system design, including problems related to security, quality of service, performance, manageability, and more. Leading researchers Dimitrios Serpanos and Tilman Wolf develop architectures for all network sub-systems, bridging the gap between operation and VLSI. This book provides comprehensive coverage of the technical aspects of network systems, including system-on-chip technologies, embedded protocol processing and high-performance, and low-power design. It develops a functional approach to network system architecture based on the OSI reference model, which is useful for practitioners at every level. It also covers both fundamentals and the latest developments in network systems architecture, including network-on-chip, network

processors, algorithms for lookup and classification, and network systems for the next-generation Internet. The book is recommended for practicing engineers designing the architecture of network systems and graduate students in computer engineering and computer science studying network system design. This is the first book to provide comprehensive coverage of the technical aspects of network systems, including processing systems, hardware technologies, memory managers, software routers, and more. Develops a systematic approach to network architectures, based on the OSI reference model, that is useful for practitioners at every level. Covers both the important basics and cutting-edge topics in network systems architecture, including Quality of Service and Security for mobile, real-time P2P services, Low-Power Requirements for Mobile Systems, and next generation Internet systems.

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

Addresses the Challenges Associated with System-on-Chip Integration Network-on-Chip: The Next Generation of System-on-Chip Integration examines the current issues restricting chip-on-chip communication efficiency, and explores Network-on-chip (NoC), a promising alternative that equips designers with the capability to produce a scalable, reusable, and high-performance communication backbone by allowing for the integration of a large number of cores on a single system-on-chip (SoC). This book provides a basic overview of topics associated with NoC-based design: communication infrastructure design, communication methodology, evaluation framework, and mapping of applications onto NoC. It details the design and evaluation of different proposed NoC structures, low-power techniques, signal integrity and reliability issues, application mapping, testing, and future trends. Utilizing examples of chips that have been implemented in industry and academia, this text presents the full architectural design of components verified through implementation in industrial CAD tools. It describes NoC research and developments, incorporates theoretical proofs strengthening the analysis procedures, and includes algorithms used in NoC design and synthesis.

In addition, it considers other upcoming NoC issues, such as low-power NoC design, signal integrity issues, NoC testing, reconfiguration, synthesis, and 3-D NoC design. This text comprises 12 chapters and covers: The evolution of NoC from SoC—its research and developmental challenges NoC protocols, elaborating flow control, available network topologies, routing mechanisms, fault tolerance, quality-of-service support, and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low-power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application-specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network-on-Chip: The Next Generation of System-on-Chip Integration covers the basic topics, technology, and future trends relevant to NoC-based design, and can be used by engineers, students, and researchers and other industry professionals interested in computer architecture, embedded systems, and parallel/distributed systems.

The demand for mobile broadband will continue to increase in upcoming years, largely driven by the need to deliver ultra-high definition video. 5G is not only evolutionary, it also provides higher bandwidth and lower latency than the current-generation technology. More importantly, 5G is revolutionary in that it is expected to enable fundamentally new applications with much more stringent requirements in latency and bandwidth. 5G should help solve the last-mile/last-kilometer problem and provide broadband access to the next billion users on earth at a much lower cost because of its use of new spectrum and its improvements in spectral efficiency. 5G wireless access networks will need to combine several innovative aspects of decentralized and centralized allocation looking to maximize performance and minimize signaling load. Research is currently conducted to understand the inspirations, requirements, and the promising technical options to boost and enrich activities in 5G. Design Methodologies and Tools for 5G Network Development and Application presents the enhancement methods of 5G communication, explores the methods for faster communication, and provides a promising alternative solution that equips designers with the capability to produce high performance, scalable, and adoptable communication protocol. This book provides complete design methodologies, supporting tools for 5G communication, and innovative works. The design and evaluation of different proposed 5G structures signal integrity, reliability, low-power techniques, application mapping, testing, and future trends. This book is ideal for researchers who are working in communication, networks, design and implementations, industry personnel, engineers, practitioners, academicians, and students who are interested in the evolution, importance, usage, and technology adoption for 5G applications. This book covers key concepts in the design of 2D and 3D Network-on-Chip interconnect. It highlights design challenges and discusses fundamentals of NoC technology, including architectures, algorithms and tools. Coverage focuses on topology exploration for both 2D and 3D NoCs, routing algorithms, NoC router design, NoC-based system integration, verification and testing, and NoC reliability. Case studies are used to illuminate new design methodologies.

[2]. The Cell Processor from Sony, Toshiba and IBM (STI) [3], and the Sun UltraSPARC T1 (formerly codenamed Niagara) [4] signal the

growing popularity of such systems. Furthermore, Intel's very recently announced 80-core TeraFLOP chip [5] exemplifies the irreversible march toward many-core systems with tens or even hundreds of processing elements. 1.2 The Dawn of the Communication-Centric Revolution The multi-core thrust has ushered the gradual displacement of the computati- centric design model by a more communication-centric approach [6]. The large, sophisticated monolithic modules are giving way to several smaller, simpler p- cessing elements working in tandem. This trend has led to a surge in the popularity of multi-core systems, which typically manifest themselves in two distinct incarnations: heterogeneous Multi-Processor Systems-on-Chip (MPSoC) and homogeneous Chip Multi-Processors (CMP). The SoC philosophy revolves around the technique of Platform-Based Design (PBD) [7], which advocates the reuse of Intellectual Property (IP) cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations. The appeal of such a modular approach lies in the substantially reduced Time-To- Market (TTM) incubation period, which is a direct outcome of lower circuit complexity and reduced design effort. The whole system can now be viewed as a diverse collection of pre-existing IP components integrated on a single die.

This book provides comprehensive coverage of Network-on-Chip (NoC) security vulnerabilities and state-of-the-art countermeasures, with contributions from System-on-Chip (SoC) designers, academic researchers and hardware security experts. Readers will gain a clear understanding of the existing security solutions for on-chip communication architectures and how they can be utilized effectively to design secure and trustworthy systems.

This book outlines a set of issues that are critical to all of parallel architecture--communication latency, communication bandwidth, and coordination of cooperative work (across modern designs). It describes the set of techniques available in hardware and in software to address each issues and explore how the various techniques interact.

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R & D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years.

Integrated System-Level Modeling of Network-on-Chip Enabled Multi-Processor Platforms first gives a comprehensive update on recent developments in the area of SoC platforms and ESL design methodologies. The main contribution is the rigorous definition of a framework for modeling at the timing approximate level of abstraction. Subsequently this book presents a set of tools for the creation and exploration of timing approximate SoC platform models.

As the number of processor cores and IP blocks integrated on a single chip is steadily growing, a systematic approach to design the

communication infrastructure becomes necessary. Different variants of packed switched on-chip networks have been proposed by several groups during the past two years. This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces. It also provides a guideline and vision about the direction this field is moving to. Moreover, the book outlines the consequences of adopting design platforms based on packet switched network. The consequences may in fact be far reaching because many of the topics of distributed systems, distributed real-time systems, fault tolerant systems, parallel computer architecture, parallel programming as well as traditional system-on-chip issues will appear relevant but within the constraints of a single chip VLSI implementation.

The design of today's semiconductor chips for various applications, such as telecommunications, poses various challenges due to the complexity of these systems. These highly complex systems-on-chips demand new approaches to connect and manage the communication between on-chip processing and storage components and networks on chips (NoCs) provide a powerful solution. This book is the first to provide a unified overview of NoC technology. It includes in-depth analysis of all the on-chip communication challenges, from physical wiring implementation up to software architecture, and a complete classification of their various Network-on-Chip approaches and solutions. * Leading-edge research from world-renowned experts in academia and industry with state-of-the-art technology implementations/trends * An integrated presentation not currently available in any other book * A thorough introduction to current design methodologies and chips designed with NoCs

"As semiconductor technologies continues to scale, more and more cores are being integrated on the same multicore chip. This increase in complexity poses the challenge of efficient data transfer between these cores. Several on-chip network architectures are proposed to improve the design flexibility and communication efficiency of such multicore chips. However, in a larger system consisting of several multicore chips across a board or in a System-in-Package (SiP), the performance is limited by the communication among and within these chips. Such systems, most commonly found within computing modules in typical data center nodes or server racks, are in dire need of an efficient interconnection architecture. Conventional interchip communication using wireline links involve routing the data from the internal cores to the peripheral I/O ports, travelling over the interchip channels to the destination chip, and finally getting routed from the I/O to the internal cores there. This multihop communication increases latency and energy consumption while decreasing data bandwidth in a multichip system. Furthermore, the intrachip and interchip communication architectures are separately designed to maximize design flexibility. Jointly designing them could, however, improve the communication efficiency significantly and yield better solutions. Previous attempts at this include an all-photonic approach that provides a unified inter/intra-chip optical network, based on recent progress in nano-photonic technologies. Works on wireless inter-chip interconnects successfully yielded better results than their wired counterparts, but their scopes were limited to establishing a single wireless connection between two chips rather than a communication architecture for a system as a whole. In this thesis, the design of a seamless hybrid wired and wireless interconnection network for multichip systems in

a package is proposed. The design utilizes on-chip wireless transceivers with dimensions spanning up to tens of centimeters. It manages to seamlessly bind both intrachip and interchip communication architectures and enables direct chip-to-chip communication between the internal cores. It is shown through cycle accurate simulations that the proposed design increases the bandwidth and reduces the energy consumption when compared to the state-of-the-art wireline I/O based multichip communications."--Abstract.

The next generation of computer system designers will be less concerned about details of processors and memories, and more concerned about the elements of a system tailored to particular applications. These designers will have a fundamental knowledge of processors and other elements in the system, but the success of their design will depend on the skills in making system-level tradeoffs that optimize the cost, performance and other attributes to meet application requirements. This book provides a new treatment of computer system design, particularly for System-on-Chip (SOC), which addresses the issues mentioned above. It begins with a global introduction, from the high-level view to the lowest common denominator (the chip itself), then moves on to the three main building blocks of an SOC (processor, memory, and interconnect). Next is an overview of what makes SOC unique (its customization ability and the applications that drive it). The final chapter presents future challenges for system design and SOC possibilities.

A presentation of state-of-the-art approaches from an industrial applications perspective, Communication Architectures for Systems-on-Chip shows professionals, researchers, and students how to attack the problem of data communication in the manufacture of SoC architectures. With its lucid illustration of current trends and research improving the performance, quality, and reliability of transactions, this is an essential reference for anyone dealing with communication mechanisms for embedded systems, systems-on-chip, and multiprocessor architectures—or trying to overcome existing limitations. Exploring architectures currently implemented in manufactured SoCs—and those being proposed—this book analyzes a wide range of applications, including: Well-established communication buses Less common networks-on-chip Modern technologies that include the use of carbon nanotubes (CNTs) Optical links used to speed up data transfer and boost both security and quality of service (QoS) The book's contributors pay special attention to newer problems, including how to protect transactions of critical on-chip information (personal data, security keys, etc.) from an external attack. They examine mechanisms, revise communication protocols involved, and analyze overall impact on system performance.

Foreword -- Foreword to the First Printing -- Preface -- Chapter 1 -- Introduction -- Chapter 2 -- Message Switching Layer -- Chapter 3 -- Deadlock, Livelock, and Starvation -- Chapter 4 -- Routing Algorithms -- Chapter 5 -- CollectiveCommunicationSupport -- Chapter 6 -- Fault-Tolerant Routing -- Chapter 7 -- Network Architectures -- Chapter

8 -- Messaging Layer Software -- Chapter 9 -- Performance Evaluation -- Appendix A -- Formal Definitions for Deadlock Avoidance -- Appendix B -- Acronyms -- References -- Index.

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